

**S/N Unknown**

**PATENT**

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicant:	Sunil Talwar et al.	Examiner:	Unknown
Serial No.:	Unknown	Group Art Unit:	Unknown
Filed:	Even Date Herewith	Docket:	1365.065US1
Title:	LOGIC CIRCUITS FOR PERFORMING THRESHOLD FUNCTIONS		

---

**INFORMATION DISCLOSURE STATEMENT**

MS Patent Application  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 *et. seq.*, the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicants respectfully request that this Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicants request that a copy of the 1449 form, initialed as being considered by the Examiner, be returned to the Applicants with the next official communication.

Pursuant to 37 C.F.R. §1.97(b), it is believed that no fee or statement is required with the Information Disclosure Statement. However, if an Office Action on the merits has been mailed, the Commissioner is hereby authorized to charge the required fees to Deposit Account No. 19-0743 in order to have this Information Disclosure Statement considered.

The Examiner is invited to contact the Applicants' Representative at the below-listed telephone number if there are any questions regarding this communication.

The present application is either a U.S. national patent application filed after June 30, 2003 or an international application that entered the national stage under 35 U.S.C. § 371 after June 30, 2003. Thus, Applicant believes that the U.S. Patent & Trademark Office has waived the requirement under 37 C.F.R. 1.98 (a)(2)(i) for submitting a copy of each cited U.S. patent and each U.S. patent application publication. The waiver is provided in a pre-OG notice from the U.S. Patent & Trademark Office entitled "Information Disclosure Statements May Be Filed Without Copies of U.S. Patents and Published Applications in Patent Applications filed after June 30, 2003" and dated July 11, 2003. Applicant acknowledges the requirement to submit copies of foreign patent documents and non-patent literature in accordance with 37 C.F.R. 1.98(a)(2).

Respectfully submitted,

SUNIL TALWAR ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.  
P.O. Box 2938  
Minneapolis, MN 55402  
(612) 349-9587

Date

11 Feb '04

By



Timothy B Chase  
Reg. No. 46,957

"Express Mail" mailing label number: EV332580967US

Date of Deposit: February 11, 2004

This paper or fee is being deposited on the date indicated above with the United States Postal Service pursuant to 37 CFR 1.10, and is addressed to The Commissioner for Patents, Mail Stop Patent Application, P.O. Box 1450, Alexandria, VA 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449A/PTO

**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Complete if Known

Applicati n Numb r	Unknown
Filing Dat	Even Date Herewith
First Nam d Inv ntor	Talwar, Sunil
Gr up Art Unit	Unknown
Examiner Name	Unknown

Sheet 1 of 3

Attorney Docket No: 1365.065US1

**US PATENT DOCUMENTS**

Examiner Initial *	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	Filing Date If Appropriate
	US-2002/0026465	02/28/2002	Rumynin, D , et al.	708	210	01/25/2001
	US-2002/0078110	06/20/2002	Rumynin, D , et al.	708	210	07/27/2001
	US-2,475,250	08/07/1981	Jean-Pierre Houdard, , et al.	G06F	7/38	
	US-3,634,658	01/11/1972	Brown, Richard	235	92LG	03/19/1970
	US-3,757,098	09/04/1973	Wright, Carl	235	175	05/12/1972
	US-4,399,517	08/16/1983	Niehaus, Jeffrey A., et al.	364	784	03/19/1981
	US-4,596,256	06/24/1986	Ascher, Gilles , et al.	128	710	01/26/1984
	US-4,607,176	08/19/1986	Burrows, James , et al.	307	449	08/22/1984
	US-4,993,421	02/19/1991	Thornton, William	128	670	07/20/1990
	US-5,095,457	03/10/1992	Ho-sun Jeong,	364	758	02/01/1990
	US-5,095,547	03/17/1992	Kerns, Carol S.	2	160	06/13/1991
	US-5,175,862	12/29/1992	Phelps, Andrew , et al.	395	800	06/11/1990
	US-5,187,679	02/16/1993	Vassiliadis, Stamatis , et al.	364	786	06/05/1991
	US-5,325,320	06/28/1994	Chiu, Chiao-Er A.	364	760	05/01/1992
	US-5,343,417	08/30/1994	Flora, Laurence P.	364	758	11/20/1992
	US-5,497,342	03/05/1996	Mou, , et al.	364	786	11/09/1994
	US-5,524,082	06/04/1996	Horstmann, P. , et al.	364	489	06/28/1991
	US-5,964,827	10/12/1999	Ngo, Hung C., et al.	708	710	11/17/1997
	US-5,995,029	11/30/1999	Ryu, Myung	341	101	10/29/1997
	US-6,023,566	02/08/2000	Belkhale, K. , et al.	395	500.03	04/14/1997
	US-617,585,2 B1	01/16/2001	Dhong, , et al.			07/13/1998
	US-626,938,6 B1	07/31/2001	Siers, , et al.			10/14/1998
	US-6,490,608	12/03/2002	Zhu, Jay	708	626	12/09/1999

**FOREIGN PATENT DOCUMENTS**

Examiner Initials*	Foreign Document No	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	T <sup>2</sup>
	EP-0168650	01/22/1986	Darringer, J. , et al.	G06F	15/60	
	EP-0309292	03/29/1989	Nishiyama, T. , et al.	G06F	15/60	

EXAMINER

DATE CONSIDERED

Substitute Disclosure Statement Form (PTO-1449)

\* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449A/PTO  
**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT**  
(Use as many sheets as necessary)

Complete if Known

Applicati n Number	Unknown
Filing Dat	Even Date Herewith
First Nam d Inv ntor	Talwar, Sunil
Group Art Unit	Unknown
Examiner Name	Unknown

Sheet 2 of 3

Attorney Docket No: 1365.065US1

**FOREIGN PATENT DOCUMENTS**

Examiner Initials*	Foreign Document No	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	T <sup>2</sup>
	EP-0442356	08/21/1991	Chang, Yen C.			
	EP-0741354	11/06/1996	Ichikawa, Takeshi	G06F	7/50	
	FR-2475250	08/07/1981	Houdard, Jean-Pierre , et al.	606F	7/38	
	GB-2016181	09/19/1979	Gajski, Daniel	606F	7/39	
	GB-2062310	05/20/1981	Ohhashi, Masahide , et al.	606F	7/52	
	GB-2365636	02/20/2002	Rumynin, D , et al.	G06F	7/60	
	GB-2365637	02/20/2002	Dmitriy, R	G06F	7/60	
	WO-02/12995	02/14/2002	Meulemans, P	G06F	7/00	
	WO-99/22292	05/06/1999	Verbauwhede, Ingrid			

**OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS**

Examiner Initials*	Cite No <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
		BOOTH, ANDREW , "A Signed Binary Multiplication Technique", <u>Oxford University Press</u> , Reprinted from Q.J. Mech. Appl. Math. 4:236-240,(1951),Pgs. 100-104	
		CHAKRABORTY, S. , et al., "Synthesis of Symmetric Functions for Path-Delay Fault Testability", <u>12th International Conference on VLSI Design</u> , (1999),pp. 512-517	
		DADDA, L. , "On Parallel Digital Multipliers", <u>Associazione Elettrotecnica ed Elettronica Italiana</u> , Reprinted from Alta Freq. 45:574-580,(1976),Pgs. 126-132	
		DADDA, L. , "Some Schemes For Parallel Multipliers", <u>Associazione Elettrotecnica ed Elettronica Italiana</u> , Reprinted from Alta Freq. 34:349-356,(1965),Pgs. 118-125	
		DEBNATH, D. , "Minimization of AND-OR-EXOR Three-Level Networks with AND Gate Sharing", <u>IEICE Trans. Inf. &amp; Syst.</u> , E80-D, 10, (1997),pp. 1001-1008	
		DRECHSLER, R. , et al., "Sympathy: Fast Exact Minimization of Fixed Polarity Reed-Muller Expressions for Symmetric Functions", <u>IEEE ED&amp;TC 1995, Proceedings European Design and Test Conference</u> , (March 6-9, 1995),91-97	
		DRECHSLER, R. , et al., "Sympathy: Fast Exact Minimization of Fixed Polarity Reed-Muller Expressions for Symmetric Functions", <u>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</u> , 16(1), (1997),pp. 1-5	
		FLEISHER, H. , "Combinatorial Techniques for Performing Arithmetic and Logical Operations", <u>IBM Research Center, RC-289, Research Report</u> , (July 18, 1960),1-20	
		FOSTER, CAXTON , et al., "Counting Responders in an Associative Memory", <u>The Institute of Electrical and Electronics Engineers, Inc.</u> , Reprinted, with permission, from IEEE Trans. Comput. C-20:1580-1583,(1971),Pgs. 86-89	

EXAMINER

DATE CONSIDERED

Substitute Disclosure Statement Form (PTO-1449)

\* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449A/PTO

**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Complete if Known

Applicati n Number	Unknown
Filing Dat	Even Date Herewith
First Nam d Inv ntor	Talwar, Sunil
Group Art Unit	Unknown
Examiner Name	Unknown

Sheet 3 of 3

Attorney Docket No: 1365.065US1

**OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS**

Examiner Initials*	Cite No <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
		GOTO, et al., "A 54 x 54-b Regularly Structured Tree Multiplier", <u>IEEE Journal of Solid-State Circuits</u> , Vol 27, No. 9, (Sept. 1992),1229-1236	
		HEKSTRA, et al., "A Fast Parallel Multiplier Architecture", <u>IEEE International Symposium on Circuits and Systems; Institute of Electrical and Electronic Engineers</u> , c1977-c1996, 20v. :ill. :28cm, (1992),2128-2131	
		HO, IRVING, et al., "Multiple Addition by Residue Threshold Functions and Their Representation by Array Logic", <u>The Institute of Electrical and Electronics Engineers, Inc., Trans. Comput. C-22:762-767</u> , (1973),80-85	
		JONES, ROBERT, et al., "Parallel Counter Implementation", <u>Conf. Rec. 26th Asilomar Conf. Signals, Systems &amp; Computers</u> , Vol. 1, ISBN 0-8186-3160-0,(1992),pp. 381-385	
		NIENHAUS, H., "Efficient Multiplexer Realizations of Symmetric Functions", <u>IEEE</u> , (1981),pp. 522-525	
		OKLOBDZIJA, V G., et al., "Improving multiplier design by using improved column compression tree and optimized final adder in CMOS technology", <u>IEEE transactions on Very Large Scale Integration (VLSI) Systems</u> , IEEE, Inc, New York, vol. 3, no. 2,(1995),292-301	
		SWARTZLANDER JR., E E., "Parallel Counters", <u>IEEE Transactions on Computers</u> , C-22(11), (November 1973),1021-1024	
		VASSILIADIS, S., et al., "7/2 Counters and Multiplication with Threshold Logic", <u>IEEE</u> , (1997),pp. 192-196	
		WALLACE, C., "A Suggestion for a Fast Multiplier", <u>The Institute of Electrical and Electronics Engineers, Inc., Reprinted, with permission, from IEEE Trans. Electron. Comput. EC-13:14-17</u> , (1964),114-117	
		ZURAS, D, et al., "Balanced delay trees and combinatorial division in VLSI", <u>IEEE Journal of Solid State Circuits</u> , SC-21, IEEE Inc, New York, Vol. SC-21, no. 5,(1986),814-819	

EXAMINER

DATE CONSIDERED

Substitute Disclosure Statement Form (PTO-1449)

\* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. <sup>1</sup> Applicant's unique citation designation number (optional) <sup>2</sup> Applicant is to place a check mark here if English language Translation is attached